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HfS_2 Electron Double Layer Transistor with High Drain Current

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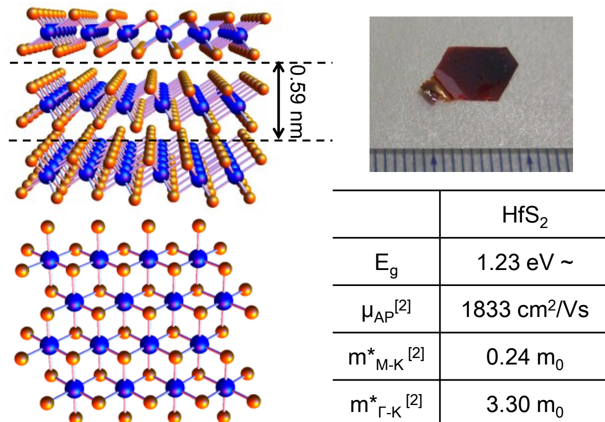
Abstract

Hafnium disulfide (HfS_2) is an uninvestigated transition metal dichalcogenide (TMD) which is expected to have the high electron mobility and the reasonable bandgap. In this report, we focused on the evaluation of potential of HfS_2 for field effect devices. To avoid the degradation of mobility due to the interface between HfS_2 and substrate, we introduce the electric double layer (EDL) transistor structure using electrolyte gel for the gate contact. The device shows substantial enhancement of drain current modulation compared to the back-gate operation. The results suggest the superior transport characteristics of HfS_2 atomically thin layers.

1. Introduction

TMDs are analogues of graphene with intrinsic finite bandgap. MoS_2, which is the most studied TMD, shows superior off current characteristics with current on/off ratio of ~10^8 and electron mobility of over 200 cm^2/Vs[1]. However, higher electron mobility is required for applications with low supply voltage and high current operation. HfS_2 is one of the TMDs, which has octahedral coordinate crystal structure and is expected to have a high acoustic phonon limited mobility (μ_{AP}) as shown in Fig. 1. Previously, we firstly reported the current properties of HfS_2 channel transistor using Al_2O_3/p^+-Si back gate structure and the channel thickness of less than 7 nm[3]. The results showed robust current saturation and ohmic like contact of S/D electrodes. However, the drain current was not high enough (> 0.3 μA/μm) to be useful for high-speed logic applications. The reason of low drain current can be assumed to be due to interface or bulk traps of atomic layer deposited (ALD) Al_2O_3 back-gate insulator. They interrupt the electric field and decrease the carrier density in HfS_2 channel. In this report, we introduced the EDL gate structure to reduce the effect of HfS_2/Al_2O_3 interface and evaluate the potential of HfS_2 channel. Polyethylene oxide (PEO) and $LiClO_4$ mixture[4] was used as electrolyte gel for the EDL formation.



	HfS_2
E_g	1.23 eV ~
μ_{AP} [2]	1833 cm^2/Vs
$m^*_{M\text{-}K}$ [2]	0.24 m_0
$m^*_{\Gamma\text{-}K}$ [2]	3.30 m_0

Fig. 1 Crystal structure, bulk peace, and expected physical properties of HfS_2.

2. Device Fabrication and Structure

We used the commercially supplied highly oriented and pure bulk HfS_2 piece for device fabrication. At first, 75-nm-thick Al_2O_3 was deposited on degenerately doped Si substrate by ALD with TMA/H_2O. Then, HfS_2 flakes are transferred on to Al_2O_3 by mechanical exfoliation using scotch tape. Secondly, Ti/Au S/D contacts were fabricated by electron beam (EB) lithography and EB evaporation. Then, Cr/Au back gate electrode was formed by evaporation. After the back-gate FET measurements, preparation of electrolyte gel was carried out. Polyethylene oxide (PEO) and $LiClO_4$ were diluted to 20 mg/ml by methanol and 10 mg/ml by deionized water, respectively. Then, they were agitated by stirrer for one hour. These two solutions were mixed together in the ratio of 1:1 and stirred again. Finally, the preparation was poured over the substrate followed by baking on hotplate at 90 °C for 30 min.

The schematic image of fabricated device structure is shown in Fig. 2. Probes were contacted to source drain electrodes formed on the HfS_2 flake by penetrating the Electrolyte gel layer. Another probe was set on metals without connecting to the HfS_2 and other electrodes. Each three electrodes and HfS_2 channel were uniformly covered

by the electrolyte gel. Li^+ ions are drawn close to the surface of channel and aligned when a positive bias is applied to an isolated gate pad. In the semiconductor channel, electrons are also aligned against Li^+ ions in electrolyte. The thickness of electron-Li^+ layer, which defines the capacitance of EDL gate, is considered to be 1~5 nm. This very thin EDL can realize the large gate capacitance and efficient gate modulation.

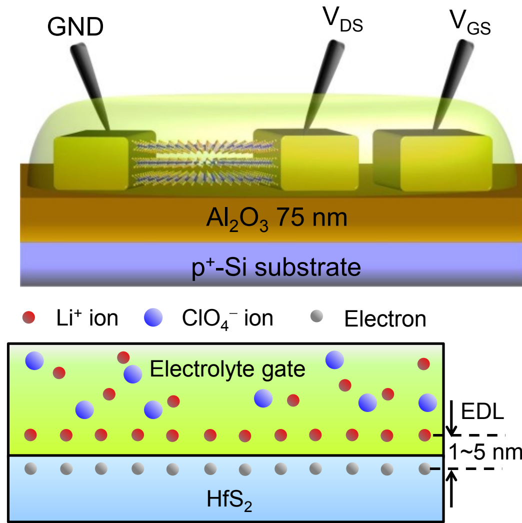


Fig. 2 Schematic image of HfS_2 electric double layer transistor and electric double layer

3. Results and Discussion

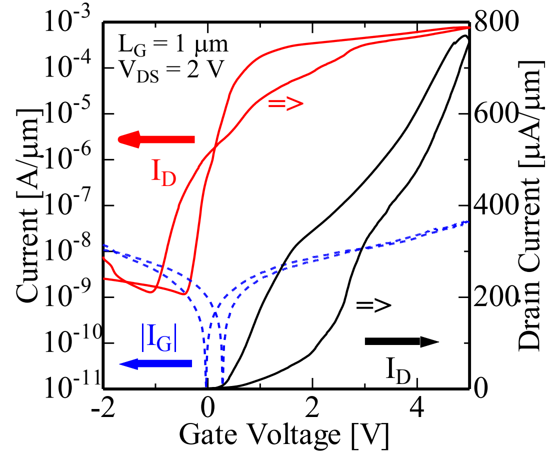
Transfer (I_D-V_{GS}) characteristics of fabricated device structure are shown in Fig. 3 (a) EDL transistor and (b) back-gate transistor (before electrolyte gate formation) for the same device. In the logarithmic plot (red solid line) for EDL transistor, drain current indicated that the on/off ratio was more than 10^5 which was limited by gate leakage current I_G. The subthreshold slope (SS) of <200 mV/dec was obtained, although the hysteresis was observed. The hysteresis in current probably depends on the response of ion transport and residual traps at the interface. The I_g (blue dashed line) was small enough than I_D for positive bias and the critical break down of insulation did not occur for electrolyte.

According to the linear plot (black solid line), the maximum drain current was 0.75 mA/μm with the L_G = 1 μm at the V_{DS} of 2 V. The maximum I_D is over 1000 times larger than that observed for back gate operation. This significant enhancement might be caused by the increase of gate capacitance and improvement of interface properties compared with back-gate structure.

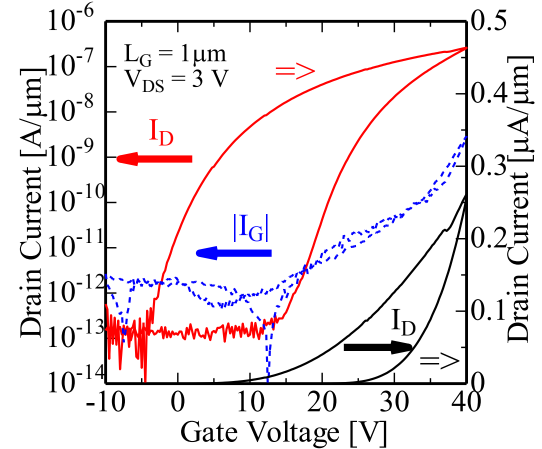
The extracted low-field effective mobility (μ_{eff}) from the I_D-V_{GS} curves for EDL transistor at the V_{DS} of 50 mV (not shown) is at least 16~80 cm^2/Vs from the typical equation as follows

$$\mu_{eff} = \frac{\partial I_D}{\partial V_{GS}} \frac{L}{W C_{OX}} \frac{1}{V_{DS}}$$

The μ_{eff} is also substantially increased compared with the mobility estimated from the back-gate devices (~0.1 cm^2/Vs). However, these values still have many components which cause the underestimation of mobility such as the effect of series resistance, inefficient field effect due to the long distance between channel and gate contact and small contact area between gate pad and electrolyte. Therefore, the optimization of device design and measurement scheme would obtain the correct and higher mobility.



(a) transfer characteristics of EDL transistor



(b) transfer characteristics of back-gate transistor

Fig. 3 I-V characteristics of EDL and back-gated transistor

4. Conclusions

To summarize, a HfS_2 EDL transistor was fabricated by using PEO:$LiClO_4$ electrolyte gel as gate for evaluation of electron-transport ability of HfS_2 thin layers. The I_D-V_{GS} characteristics indicated 100~1000 times increase of on current and extracted effective mobility compared with Al_2O_3 back gate devices. Although there are some uncertainty in the properties, it indicated the superior capability of EDL structure and potential of HfS_2 channel.

References

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