

# Compact InP-based 1×2 MMI Splitter on Si Substrate with BCB Wafer Bonding for Membrane Photonic Circuits

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**Abstract** — Ultra-low power and compact optical interconnects can be realized with III-V-based membrane photonic integrated circuits (PICs) on Si platform. This study focused design and fabrication of the III-V-based passive components of the PICs, especially, a compact 1×2 multimode interference (MMI) splitter with SiO<sub>2</sub> buried GaInAsP wire structure. The calculated excess loss was as low as 0.28dB in the optimized structure, and the structural tolerance obtained was as low as 0.05dB, when MMI width  $W_{\text{MMI}}$ , length  $L_{\text{MMI}}$ , output gap  $Y$  were changed in range of  $\pm 50$  nm. The footprint of the MMI region was only  $1.4 \times 1.5 \mu\text{m}^2$ . In the spectral range of 1548-1552 nm, the average excess loss measured was around 3dB and the average imbalance between the outputs was 0.5dB allowing the compact size and light splitting function.

**Index terms** — Multimode interference (MMI), III-V-based passive components, membrane photonic integrated circuits (PICs), optical beam splitters.

## I. INTRODUCTION

The processing speed in large-scale integrated circuits (LSIs) is being limited by the RC time constant and the power consumption on the global electrical wires [1-2]. As one solution, optical on-chip interconnects have been proposed with the replacement of the copper wiring in Si-LSI [3-4]. To realize them, we proposed the concept of membrane photonic integrated circuits (PICs) such as shown in Fig. 1, which consist of the thin III-V-based PICs with high index-contrast structure of the semiconductor core layer sandwiched by SiO<sub>2</sub> or air claddings [5-6]. The strong optical confinement to the core layer in the membrane structure leads to ultra-compact footprints and low-power dissipation. For integration technique of III-V/Si, a Benzocyclobutene (BCB) adhesive wafer bonding was used to realize the membrane PICs by the way of backend process after the CMOS process [7]. For such III-V PICs, we have reported membrane lasers [8] and photo-detectors [9] as active components. InP-based wire waveguides on the Si substrate was also reported with a propagation loss of 4 dB/cm [10].

For membrane PICs, passive devices for splitting and coupling of the optical signals are necessary. As such a beam splitter, N×N multi-mode interference (MMI) devices have been extensively investigated due to its simple structure and large fabrication tolerance [11-12]. So far, an InP-based 1×2 MMI splitter on Si substrate was reported, but the footprint was rather larger to  $2.75 \times 6.64 \mu\text{m}^2$  [13].

One of the advantages of this index contrast membrane

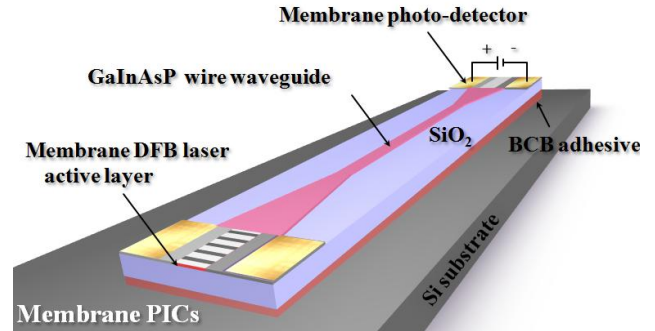


Fig. 1 Schematic representation of a membrane photonic integrated circuits consisting of the membrane DFB laser, the GaInAsP wire waveguide and the membrane photo-detector.

structure is the compactness of components. A 1×2 MMI splitter on Si-on-insulator (SOI) substrate was reported with its compact size ( $1.8 \times 2.6 \mu\text{m}^2$ ) and low excess loss (0.45dB) structure [14]. Since the index contrast of our InP-based membrane structure is comparable to SOI, similar size InP-based MMI splitter should be realized.

In this study, we focused on design and fabrication of an ultra-compact (to extent of the MMI on SOI) GaInAsP 1×2 MMI splitter with SiO<sub>2</sub> buried wire structure which can be integrated with the light sources for membrane PICs.

## II. DESIGN

A 3dB splitter, 1×2 MMI structure consisting of one input waveguide, one MMI region, and two output waveguides was theoretically investigated, where the GaInAsP 1×2 MMI splitter was assumed to be buried in 1.5- $\mu\text{m}$ -thick SiO<sub>2</sub> upper and bottom claddings on Si substrate by BCB wafer bonding as shown in Fig. 2 (a).

In the calculation, finite difference method (FDM) was used by assuming transverse electric (TE) polarization with the wavelength fixed at 1550 nm. The refractive indices of GaInAsP and SiO<sub>2</sub> were assumed to be 3.35 and 1.45, respectively. While the size of MMI region was designed for compact and low-loss structure, the sizes of the input and the output waveguides were set to be 500-nm-wide and 150-nm-thick, satisfying the singlemode condition at 1550 nm wavelength with the equivalent refractive index  $n_{\text{eq}}$  2.0 of the GaInAsP wire waveguide. Figure 2(b) illustrates a top view of the MMI splitter model used for the FDM

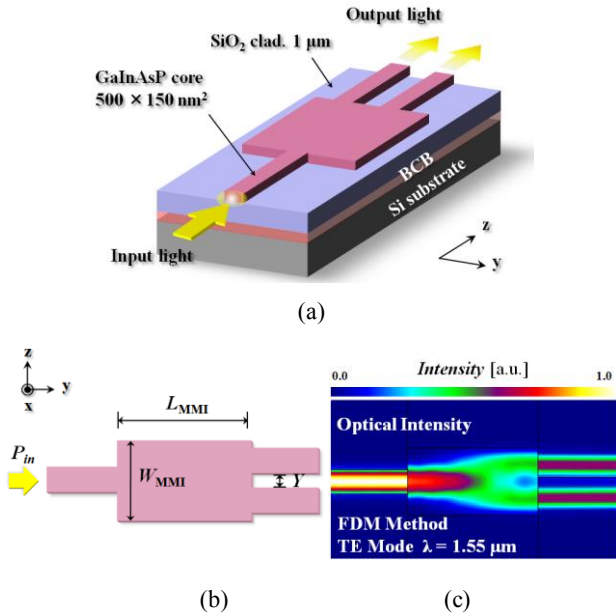


Fig. 2 (a) Schematic structure of the MMI splitter; (b) Top view of the FDM calculation model; (c) launched TE polarization optical intensity.

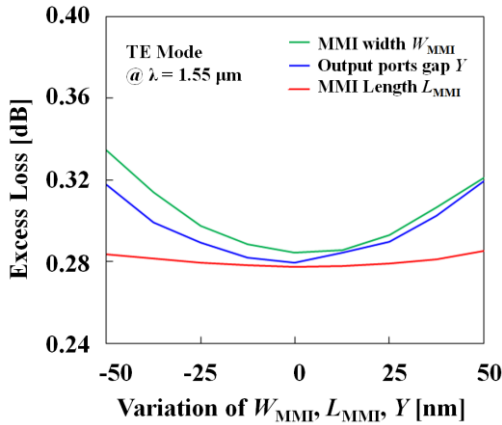


Fig. 3 Estimated structure tolerance by considering excess loss versus MMI width  $W_{\text{MMI}}$ , output ports gap  $Y$  and MMI length  $L_{\text{MMI}}$ .

simulation. The parameters of MMI region were set as MMI width  $W_{\text{MMI}}$ , length  $L_{\text{MMI}}$ , and the gap between output ports  $Y$ . The excess loss of  $1 \times 2$  MMI was calculated from the ratio of total output power of both ports to the input power. By changing the above mentioned parameters,  $1 \times 2$  MMI structure for compact and low-loss property was investigated. The minimum excess loss of 0.28 dB was obtained when the parameters were  $W_{\text{MMI}} = 1.41 \mu\text{m}$ ,  $L_{\text{MMI}} = 1.54 \mu\text{m}$ , and  $Y = 0.20 \mu\text{m}$ . Figure 2(c) shows the calculated optical intensity with TE polarization, which was launched into the input GaInAsP wire waveguide of the MMI splitter with the optimized structure.

Considering fabrication error caused by process variations, the fabrication tolerance was also estimated by changing each parameter in the range of  $\pm 50$  nm (which can be regarded as the maximum deviation of our fabrication process by using an electron-beam-lithography followed by

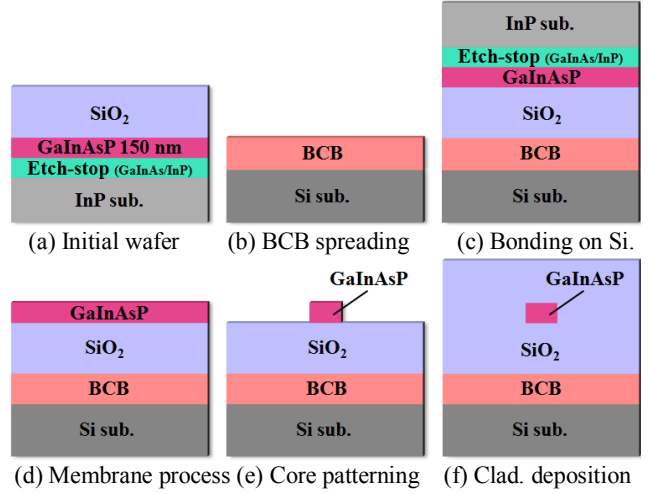


Fig. 4 Schematics for fabrication process with GaInAsP membrane structure on Si substrate using BCB adhesive wafer bonding.

a dry etching) from the optimized structure. Figure 3 shows the excess loss as a function of the deviation from the optimum value of each parameter. As can be seen, the excess loss variation was only 0.05 dB when the width was changed, and was 0.04 dB when output ports gap was varied in the range of  $\pm 50$  nm. At the same time, the increased excess loss was as low as 0.01 dB during MMI length was also changed in the range of  $\pm 50$  nm. The  $1 \times 2$  MMI splitter size and the excess loss calculated are comparable to the value of the MMI splitter with Si wire waveguide on a SOI substrate, hence compact and low-loss optical elements could be fabricated even in the GaInAsP membrane circuits.

### III. FABRICATION

The device fabrication process was performed by the following steps as illustrated in Fig. 4, and comprised of two main steps; a BCB adhesive wafer bonding and a device structure fabrication.

For the BCB bonding process, organo-metallic vapor-phase epitaxy (OMVPE) was used to grow an initial GaInAsP/InP wafer which consists of a 150-nm-thick  $\text{Ga}_{0.21}\text{In}_{0.79}\text{As}_{0.46}\text{P}_{0.54}$  ( $\lambda_g = 1.22 \mu\text{m}$ ) core layer on top of two etch-stop layers (InP/GaInAs). Then, as shown Fig. 4(a), a 1.5- $\mu\text{m}$ -thick  $\text{SiO}_2$  bottom cladding layer was deposited on the GaInAsP/InP wafer by plasma-enhanced chemical-vapor deposition (PECVD). Meanwhile, BCB was spin-coated onto the Si wafer, and then, it was thermally pre-cured for its polymerization in  $\text{N}_2$  environment at  $210^\circ\text{C}$ . Both wafers were bonded with a bonding pressure of 5.9 kPa at  $130^\circ\text{C}$ , and completely solidified by hard-curing at  $250^\circ\text{C}$  under  $\text{N}_2$  atmosphere. With selective wet etching, the InP substrate and two etch-stop layers were removed, then GaInAsP membrane was formed on the Si substrate. Figure 5 shows the GaInAsP membrane of 2 inch wafer formed after BCB bonding and membrane process.

Next, in order to fabricate waveguides, a  $\text{SiO}_2$  hard mask

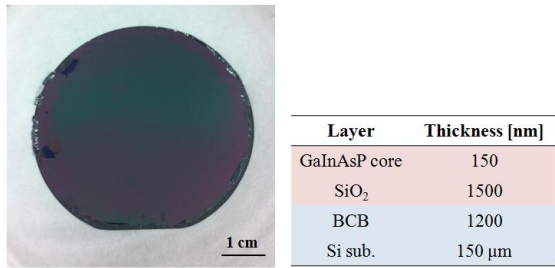


Fig. 5 Image of 2-inch GaInAsP membrane surface on a Si substrate after BCB adhesive wafer bonding and selective wet-etching of the InP substrate and etch-stop layers.

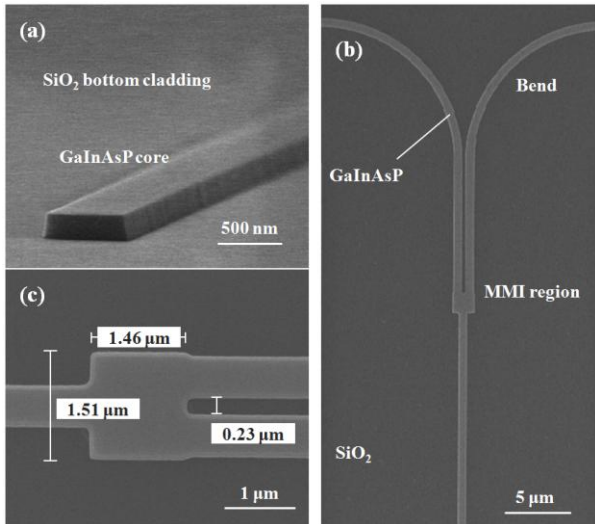


Fig. 6 SEM image of the MMI splitter (a) input waveguide on cross-sectional; (b) the MMI region and (c) enlarged micrograph on top view.

was deposited by PECVD and electron beam resist (ZEP520A/ZEP-C<sub>60</sub> double layer) was spun onto the GaInAsP membrane on the Si substrate. After forming the mask pattern using electron beam lithography, the SiO<sub>2</sub> mask was transferred by reactive-ion etching (RIE) using CF<sub>4</sub> gas. And then, the GaInAsP core layer was etched by inductively-coupled plasma RIE (ICP-RIE) using a mixture of CH<sub>4</sub> and H<sub>2</sub> gas. After each etching process, the surface was cleaned by O<sub>2</sub> plasma ashing, and SiO<sub>2</sub> mask was removed with BHF solution. Finally, to obtain the complete device structure, a 1.5-μm-thick SiO<sub>2</sub> upper cladding was deposited by PECVD. Figure 6 represents the scanning electron microscope (SEM) images of 1×2 MMI splitter fabricated; (a) side view of input port and (b) and (c) top view of device body. The width  $W_{MMI}$ , length  $L_{MMI}$  and the gap of output ports  $Y$  of the fabricated MMI were 1.46 μm, 1.51 μm, and 0.23 μm, respectively. The width and the thickness of the input and output ports were 0.49 and 0.15 μm, respectively.

#### IV. MEASUREMENTS

The measurement of fabricated MMI splitter was carried

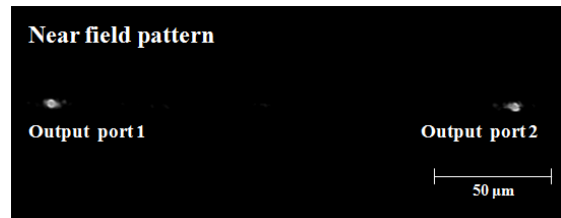


Fig. 7 Near field pattern of MMI splitter at wavelength 1.55 μm.

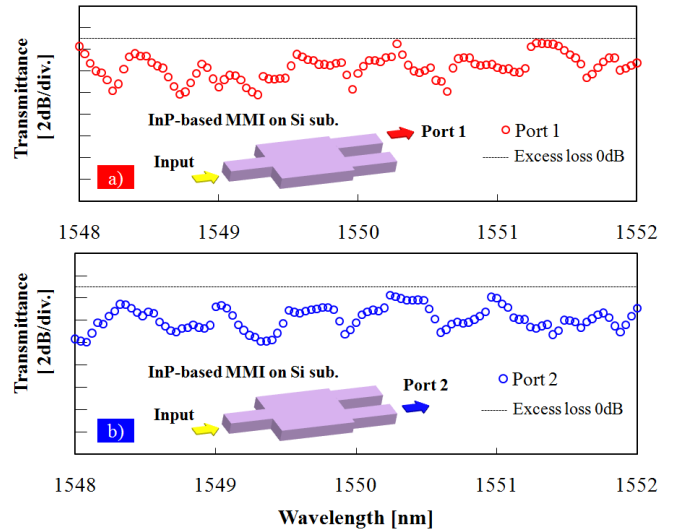


Fig. 8 Transmission of MMI splitter on Si substrate; (a) output port 1 and (b) output port 2.

out in the way that the input and outputs light beams on cleaved facets were coupled to each of the waveguide using spherical-lensed single mode fibers (mode field diameter of  $\sim 1.0$  μm). Transmission measurement was performed with a wavelength tunable laser. The light transmitted through the device was coupled to the other spherical-lensed single mode fiber and projected on an optical power detector. A polarization controller was used to maintain the transverse electric (TE) incident polarization of the input light from the light source.

Figure 7 indicates the near field pattern on cross-sectional view of upper port and lower port at 1.55 μm wavelength.

Figures 8 shows the transmission of the output port 1 and port 2 of the MMI splitter. The wavelength of input light was swept and the average excess loss was obtained to be 3dB in the range of 1548-1552 nm. The average imbalance, which defined as the power ratio of the output ports was 0.5dB in the spectral range of 1548-1552 nm. The deviation of the excess loss value from the theoretical calculation is considered to be due to the displacement of the device sizes, and imperfect symmetric structure fabricated.

#### V. CONCLUSION

In conclusion, we designed and fabricated an ultra-compact and low-loss 1×2 MMI splitter with SiO<sub>2</sub> buried GaInAsP wire structure on a Si substrate by BCB

adhesive wafer bonding. The excess loss of calculated MMI was as low as 0.28dB in optimized structure, and this structure had a good fabrication tolerance of 0.05dB when  $W_{\text{MMI}}$ ,  $L_{\text{MMI}}$ , and  $Y$  were changed in range of  $\pm 50$  nm. The footprint of fabricated  $1 \times 2$  MMI splitter was as small as  $1.51 \times 1.46 \mu\text{m}^2$ ; in consequence, this device is about 9 times smaller than the reported InP-based  $1 \times 2$  MMI splitter [13]. The average excess loss was 3dB in C-band and the imbalance between output ports was 0.5dB, but it can still be improved by reduction of its displacement and imperfect symmetry of device structure. It is confirmed that compact optical element with low-loss property can be realized even in the GaInAsP membrane circuits.

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#### REFERENCES

- [1] P. Kapur, J. P. Mc Vittie, and K. C. Saraswat, "Technology and reliability constrained future copper interconnects. I. Resistance modeling," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 590-597, Apr. 2002.
- [2] P. Kapur, G. Chandra, J. P. Mc Vittie, and K. C. Saraswat, "Technology and reliability constrained future copper interconnects. II. Performance implications," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 598-604, Apr. 2002.
- [3] D. A. B. Miller, "Rationale and challenges for optical interconnects to electronic chips," *Proc. IEEE*, vol. 88, no.6, pp. 728-749, Jun. 2000.
- [4] M. Haurylau, G. Chen, H. Chen, J. Zhang, N. A. Nelson, D. H. Albonesei, E. G. Friedman, and P. M. Fauchet "On-chip optical interconnect roadmap: challenges and critical directions," *IEEE J. Sel. Top. Quantum Electron*, vol. 12, no. 6, pp. 1699-1705, Sep. 2011.
- [5] S. Sakamoto, H. Naitoh, M. Ohtake, Y. Nishimoto, T. Maruyama, N. Nishiyama, and S. Arai, "85°C continuous-wave operation of GaInAsP/InP-membrane buried heterostructure distributed feedback laser with polymer cladding layer," *Jpn. J. Appl. Phys.* vol. 46, no. 47, pp. L1155-L1157, Nov. 2007.
- [6] S. Arai, N. Nishiyama, T. Maruyama, and T. Okumura, "GaInAsP/InP membrane lasers for optical interconnects," *IEEE J. Sel. Top. Quantum Electron*, vol. 17, no. 5, pp. 1381-1389, Sep. 2011.
- [7] Y. Maeda, J. Lee, Y. Atsumi, N. Nishiyama, and S. Arai, "Uniform BCB bonding process toward low propagation loss," *Proc. Int. Conf. Indium Phosphide and Related Materials*, P08, May 2011.
- [8] T. Okumura, T. Koguchi, H. Ito, N. Nishiyama, and S. Arai, "Injection-type GaInAsP/InP membrane buried hetero structure distributed feedback laser with wirelike active regions," *Appl. Phys. Express*, vol. 4, no. 4, pp. 042101-1-042101-3, Mar. 2011.
- [9] T. Okumura, D. Kondo, H. Ito, S. Lee, T. Amemiya, N. Nishiyama, and S. Arai, "Lateral junction waveguide-type photodiode grown on semi-insulating InP substrate," *Jpn. J. Appl. Phys.*, vol.50, no.2 pp. 020206-1-020206-3, Feb. 2011.
- [10] J. Lee, Y. Maeda, Y. Atsumi, Y. Takino, N. Nishiyama, and S. Arai, "Low-loss GaInAsP wire waveguide on Si substrate with benzocyclobutene adhesive wafer bonding for membrane photonic circuits," *Jpn. J. Appl. Phys.* vol. 51, no. 4, pp. 042201-1-042201-5, Apr. 2012.
- [11] K. Solehmainen, M. Kapulainen, M. Harjanne, and T. Aalto, "Adiabatic and multimode interference couplers on Silicon-on-insulator," *IEEE Photon. Technol. Lett.*, vol. 18, no. 21, pp. 2287-2289, Nov. 2006.
- [12] A. Hosseini, D. N. Kwong, Y. Ahang, H. Subbaraman, X. Xu, and R. T. Chen, "1xN Multimode interference beam splitter design techniques for on-chip optical interconnections," *IEEE J. Sel. Top. Quantum Electron*, vol. 17, no. 3, pp. 510-515, June 2011.
- [13] F. Bordas, G. Roelkens, R. Zhang, E. J. Geluk, F. Karota, J. J. G. M. Van Der Tol, P. J. Van Veldhoven, R. Nötzel, D. Van Thourhout, R. Baets, and M. K. Smit, "Compact passive devices in InP membrane on silicon," *35th European Conf. on Opt. Commun. (ECOC'09)*, Vienna, Austria, paper 4.2.4, Sept. 2009.
- [14] K. Suzuki, H. C. Nguyen, T. Tamanuki, F. Shinobu, Y. Saito, Y. Sakai, and T. Baba, "Slow-light based variable symbol-rate silicon photonics DQPSK receiver," *Opt. Express*. vol. 20, no. 4, pp. 4796-4804, Feb. 2012.